

Notice of References Cited		Application/Control No.	Applicant(s)/Patent Under Reexamination	
		10/822,158	BOPPANA ET AL.	
Examiner		Art Unit		Page 1 of 1
Suchin Parihar		2825		

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,769,098	07-2004	Tanaka et al.	716/2
*	B	US-7,003,738	02-2006	Bhattacharya et al.	716/1
*	C	US-6,272,668	08-2001	Teene, Andres R.	716/10
*	D	US-2002/0152449	10-2002	Lin, Chin-hsen	716/17
*	E	US-2003/0204827	10-2003	Irie, Kazuyuki	716/5
*	F	US-5,666,288	09-1997	Jones et al.	716/17
*	G	US-5,604,680	02-1997	Bamji et al.	716/8
*	H	US-6,684,377	01-2004	Barney et al.	716/10
*	I	US-6,163,877	12-2000	Gupta, Avaneendra	716/8
*	J	US-6,009,248	12-1999	Sato et al.	716/2
K	US-				
L	US-				
M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Yoshida et al. "Accurate Pre-layout Estimation of Standard Cell Characteristics". Proceedings of the 41st Annual Conference on Design Automation, pgs 208-211, June 2004
	V	Serdar et al. "AKORD: Transistor Level and Mixed Transistor/Gate Level Placement Tool for Digital Data Paths". Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design, pgs 91-97. Nov, 1999
	W	Gupta et al. "XPRESS: A Cell Layout Generator with Integrated Transistor Folding". Proceedings of the 1996 European Design and Test Conference, pgs 393-40. March, 1996
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.